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EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	8

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,217	RUSSELL ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-37* is/are allowed.

6)☒ Claim(s) *1-11 and 17-32* is/are rejected.

7)☒ Claim(s) *12-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *22 July 2003* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment/Arguments

1. This Office Action is in response to the Response/Amendment filed on July 22nd, 2003. New claims 33-37 are added. Claims 1-37 are now pending in the application.

Information Disclosure Statement

2. The application listing of information disclosure statement (IDS) submitted on March 27th, 2003 is not a proper information disclosure statement. 37 CFR 1.98(b) requires a legible copy of each U.S. and foreign patent; publication or that portion which caused it to be listed submitted for consideration by the Office. However, the information disclosure statement is being considered by the examiner.

Drawings

3. The proposed drawings were received on July 22nd, 2003. The drawing of Figure 1B is disapproved by the examiner.

The drawing is objected to because all blocks in Figure 1B should be labeled with descriptive legends based on 37 C.F.R. § 1.84(o) for supporting the objection in the Rules and M.P.E.P. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 9 is objected to because of the following informalities:

The limitation "clock/data recovery unit" in Claim 9, Line 1 is not clear what it was meant by "clock and data recovery unit" or "clock or data recovery unit".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 20-21 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** (U.S.5,917,426) in view of **Fatehi et al.** (U.S.6,600,581).

- In regard to claims 1, 20-21 and 28-30, **Yoshifuji** discloses in Figs. 1-2 and 4-5 and in the respective portions of the specification that the network system ("*signal router*") includes switch network system having a plurality of switch matrices ("*switching matrices*"), which uses to control and manage connection data signals ("*information stream*") and connection data control system, wherein the switch matrix ("*switching matrix*") has a plurality of input terminals for receiving data signals ("*first number of inputs*") and a plurality of output terminals ("*second number of outputs*") formed by first through n-th link stages connected to one another through n-

th sub-processing units and n-th sub-control units which are controlled by the main control unit and main processing unit (For example see Abstract and in Fig. 1-2; Col. 1, Lines 5-17; Col. 2, Lines 16-40); a monitoring means for detecting any disorder in the connection with the interconnection data signals ("*errors in the information stream*"; For example see Col. 2, Lines 10-15) through n-th link stages mutually connected to each other, i.e. "*by virtue*", as disclosed in Col. 2, Line 58 through Col. 3, Line 6; Col. 10, Lines 7-19; a controlling means ("*controller*") for controlling the switch matrices to connect the selected input to the selected output terminals and substituting the actual path to the new one, in detection or reception of any disorder ("*receiving error information*") in the connection with the connection data signals (For example see Col. 5, Line 11 through Col. 6, Line 28). **Yoshifuji** also discloses each sub-control unit ("*controller*") connects to a corresponding switch matrix where one of a plurality of outputs connects to one of a plurality of inputs of the other switching matrices (For example see Figs. 1-2 and 4-5).

Yoshifuji fails to specially disclose the "*error detector connecting to the outputs and controller to detect error in the information stream*". However, such implementation is known in the art.

For example, **Fatehi** discloses in Figs. 1-2, 4, 6-7 and in the respective portions of the specification about system and method for verifying that the optical signals ("*information stream*") are properly routed between inputs and outputs ("*outputs*") of the switch fabric, i.e. "*switching matrix*", (For example see Fig. 2; Col. 3, Line 46 through Col. 4, Line 12); wherein a plurality of tag read/write elements ("*error detectors*") associated with respective one of the plurality of output ports retrieve the information (For example see Fig. 4; Col. 7, Lines 31-44) at

the output ports under the control of the controller (For example see Col. 5, Line 2-11; Col. 8, Lines 42-57) so that appropriate action can be taken.

Fatehi further discloses each one of a plurality of outputs of the switch fabric is coupled to a corresponding one of a plurality of inputs of the switch fabric (For example see Figs. 1-2; Col. 8, Lines 4-22).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the tag read/write elements in the switch fabric as taught by **Fatehi** in the **Yoshifuji**'s switch matrix, by implementing the tag read/write elements at the output of the switch matrices with the motivation being to improve the ability to detect the error at the output ports and re-route the optical signals in the switch matrix.

- Regarding claims 2 and 3, **Yoshifuji** further discloses the switch matrix receives the control by the sub-control unit to change the link path, i.e. "*experiences the failure*", whenever any disorder in the connection with the interconnection data signals is detected by the route search and renewal processing unit, i.e. "*identifies the error information generated by the error detector*", through the control of the main control unit (For example see Figs. 2 and 5; Col. 10, Line 29 through Col. 12, Line 22; it is obvious that each switch matrix in each of the switch link stages are mutually connected and controlled by the sub-control means which is actuated by the main control means, i.e. "*by virtue*", changes the link path when any disorder in the connection with the interconnection data signals detects by the monitoring means as disclosed in Col. 2, Lines 16-40). **Yoshifuji** fails to disclose *each of the switch matrixes is coupled to a corresponding monitoring means*. However, such implementation is known in the art.

For example, **Fatehi** discloses that each tag read/write elements ("*error detectors*") associate with respective one of the plurality of output ports to retrieve the information (For example see Fig. 4; Col. 7, Lines 31-44) at the output ports under the control of the controller (For example see Col. 5, Line 2-11; Col. 8, Lines 42-57).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the tag read/write elements in the switch fabric as taught by **Fatehi** in the **Yoshifuji**'s switch matrix, by implementing the tag read/write elements at the output of the switch matrices with the motivation being to improve the ability to detect the error at the output ports and re-route the optical signals in the switch matrix.

- In regard to claims 4 and 5, **Yoshifuji** further discloses the main switch control unit actuates the sub-switch control unit to change the connection path, i.e. "*reconfigure*", between the selected input and output of the switch matrix at each link stages by the sequence number assigned to each individual switch matrix as disclosed in Col. 8, Lines 22-31; in response to any disorder in the connection with the interconnection data signals (For example see Figs. 4-5; Col. 10, Line 29 through Col. 12, Line 22). **Yoshifuji** fails to disclose the method of "*coupling two outputs to the input*". However, such implementation is known in the art.

For example, **Fatehi** discloses about the method of "*coupling two outputs to the input*" via the tearing down process for the connection when detecting error in the optical signals at the output ports (For example see Col. 8, Lines 15-20).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the tag read/write elements in the switch fabric as taught by

Fatehi in the **Yoshifuji**'s switch matrix, by implementing the tag read/write elements at the output of the switch matrices with the motivation being to improve the ability to detect the error at the output ports and re-route the optical signals in the switch matrix.

7. Claims 6-9, 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** in view of **Fatehi** as applied in part 6 of this Office action above, and further in view of **Al-Salameh** (U.S.6,262,820).

- Regarding claims 6-7, **Yoshifuji** in view of **Fatehi** discloses the switch network system includes switch matrices with a plurality of input ports ("*optical receivers*") and output ports ("*optical transmitters*") at each switch matrix, signal detectors connecting at the output ports ("*transmitter error detector*") for monitoring the signal in upon a failure in the connecting path and supplying the switch control signals CS ("*error information*") to the controller, a main control unit managing and controlling the change of connection paths between the input and output ports of the switch matrix at each link stage. The combination of **Yoshifuji** and **Fatehi** does disclose about the tag read/write elements at the input ports (For example see details in Fig. 2), but fails to specifically disclose about "*the receiver error detector*". However, such implementation is known in the art.

For example, **Al-Salameh** discloses in Figs. 1-2 and 4-5 and in the respective portions of the specification that the optical node ("*signal router*"), which uses to route the transmission media ("*information stream*"), comprises a switch matrix ("*switching matrix*") having a plurality of inputs A-H for receiving transmission channel inputs ("*optical receivers*") and a plurality of

outputs I-N ("*optical transmitters*") as disclosed in Col. 5, Lines 61-66; optical monitor ("*receiver error detector*") for detecting the presence or absence of input optical signal ("*errors in the information stream*") in transmission channels, i.e. "*by virtue*", generating indications and supplying the switch control signals CS ("*error information*") to the sub-controller and then to the optical switch matrix as disclosed in Col. 4, Line 66 through Col. 5, Line 12; and a main controller ("*controller*"), when receiving the CS ("*error information*"), selects an input from the plurality of inputs to an output from the plurality of outputs (For example see Figs. 4-8; Col. 5, Lines 17-37; Col. 7, Lines 23-30).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the optical monitor in the optical communication system as taught by **Al-Salameh** in the **Yoshifuji** and **Fatehi**'s switch network system, by implementing each optical monitor at each input of the switch matrix with the motivation being to improve the ability to detect the failed path and re-route the data signal at each input and output port of each switch matrix in the system.

- Regarding claims 8-9, 22 and 31, **Yoshifuji** further discloses the network and internal data memory ("*clock and data recovery unit*") check and backup the data signal at a predetermined period time (**Yoshifuji**: For example see Col. 4, Lines 11-17; Col. 14, Lines 39-42) when the error detected by the tag read/write elements at the output ports is sent back, i.e. loop-back, to the controller so that appropriate action can be taken (**Fatehi**: For example see Col. 8, Lines 15-20, Lines 61-63). The combination of **Yoshifuji** and **Fatehi** fails to teach about "*the*

error counter resets and starts the error timer when reaching a terminal value" at the input port of the switch matrix. However, such implementation is known in the art

Al-Salameh also discloses the switch matrix restores the failure by the indicating switch control SC signal set and reset ("*clearing error counter and starting error timer*") by the counter clock ("*clock and data recovery unit*") when the threshold ("*terminal value*") has been reached as disclosed in Fig. 9; Col. 9, Line 34 through Col. 10, Line 16; and the add/drop multiplexer ("*demultiplexer*") as disclosed in Figs. 2 and 12; Col. 4, Line 17 through Col. 5, Line 60.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the counter clock in the optical communication system as taught by **Al-Salameh** in the **Yoshifuji** and **Fatehi**'s switch network system, by implementing the counter clock in the **Yoshifuji** and **Fatehi**'s switch network system with the motivation being to improve the ability to detect the failed path and re-route the data signal at a predetermined time and value in the system.

8. Claims 10-11, 17-19, 23-27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yoshifuji** in view of **Fatehi et al.** as applied in part 6 of this Office action above, and further in view of **Maezawa et al** (U.S.6,145,024).

- Regarding claims 10-11, 17-19, 23-27 and 32, **Yoshifuji** in view of **Fatehi** discloses the switch network system includes switch matrices with a plurality of input ports ("*optical receivers*") and output ports ("*optical transmitters*") at each switch matrix, the tag read/write elements ("*error checkers*") connecting at the output ports for detecting the error information

and notifying the controller ("*error information*") to take the appropriate action, a main control unit managing and controlling the change of connection paths between the input and output ports of the switch matrix at each link stage. The combination of **Yoshifuji** and **Fatehi** fails to teach about "*the frame circuit*". However, such implementation is known in the art.

For example, **Maezawa** discloses in Figs. 1-5 and in the respective portions of the specification that the switching matrix device with a plurality of switching ports for transferring data in multiplex channel path mode or high speed single channel path mode of optical fiber link with optical fiber frames, i.e. "*SONET frames*" (For example see Fig. 1 and 5; it is obvious that the frames are received in a "*sequence*"), wherein the link connection control circuit detects the error such as CRC, connection or frame validity error ("*framing error*") through the SOF ("*start-of-frame*") and EOF ("*end-of-frame*") which use for the purpose of connection control (For example see Fig. 5; Col. 16, Line 21 through Col. 17, Line 5); and compares ("*comparing*") with relevant channel path as disclosed in Col. 7, Line 13-18; Col. 23, Lines 9-26; or with reserved bits in PCONF, i.e. "*B1 byte in parity entry*" (For example see Fig. 6; Col. 22, Lines 1-31) and sends the control signal ("*error information*") to the channel path control circuit for link recovery operations from error detections (For example see Figs. 2-4; Col. 14, Lines 21-54; Col. 18, Line 26 through Col. 19, Line 17).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use the frame circuit in the optical communication system as taught by **Maezawa** in the **Yoshifuji** and **Fatehi**'s switch network system, by implementing the frame circuit in the **Yoshifuji** and **Fatehi**'s switch network system with the motivation being to

improve the ability to detect the errors of the optical frames in the multiplex channel path or high speed single channel path mode.

Response to Arguments

9. Applicant's arguments filed on July 22nd, 2003 have been fully considered but they are not persuasive.

In regard to claims 1, 20 and 28, Applicant argues that the combination of **Fatehi** and **Yoshifuji** fails to disclose "*the error detector coupled to the output of the switching matrix is configured to detect errors in the information stream received by the input of the switching matrix*". Examiner respectfully disagrees. The combination of **Fatehi** and **Yoshifuji** does disclose about the switch fabric with a plurality of tag read/write elements ("*error detectors*") associated with respective one of the plurality of output ports ("*output*") for detecting the error information in the optical signals ("*information stream*") at the output ports under the control of the controller ("*controller*"), so that appropriate action can be taken as disclosed in part 6 of this Office action above. Therefore, Examiner concludes that the combination of **Fatehi** and **Yoshifuji** teaches the arguable feature.

Regarding claim 5, Applicant argues that the combination of **Fatehi** and **Yoshifuji** fails to disclose the method of "*coupling two outputs to the input*". Examiner respectfully disagrees. The combination of **Fatehi** and **Yoshifuji** does disclose about the method of "*coupling two outputs to the input*" via the tearing down process for the connection when detecting error in the

optical signals at the output ports, as disclosed in part 6 of this Office action above. Therefore, Examiner concludes that the combination of **Fatehi** and **Yoshifuji** teaches the arguable feature.

Claims 2-11, 17-19, 21-27 and 29-32 are rejected as in Parts 6-8 above of this Office action and by virtue of their dependence from claims 1, 20 and 28.

Allowable Subject Matter

10. Claims 12-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 33-37 are allowed. The following is an examiner's statement of reasons for allowance:

Claims 33-37 are considered allowable since when reading the claims in light of the specification, none of the references of record-alone or in combination disclose or suggest the combination of limitations specified in the independent claims including the integrator configured to determine and calculate the error rate based on error count during a period of time.

Substantially regarding claim 33, the prior art of record fails to disclose the signal router for routing information over the network, which comprises the switching matrix having a first number of inputs and a second number of outputs, the error detector coupled to one of the second

number of outputs and configured to generate error information by virtue of being configured to detect errors in the information stream and the controller coupled to the switching matrix and the error detector is configured to select one of the first number of inputs from the first number of inputs, receive error information from the error detector, and configure the switching matrix to couple one of the first number of inputs to one of the second number of outputs, and the switching matrix is configured to receive information stream at one of the first number of inputs, wherein the information stream comprises a plurality of frames and the error detector comprises the error checker coupled to the switching matrix and the controller is configured to generate error check information included in the error information, and the framing circuit coupled to the switching matrix, the controller, and the error checker, and configured to detect the start-of-frame condition for each one of the plurality of frames, indicate the start-of-frame condition to the error checker, detect the end-of-frame condition for each one of the plurality of frames, indicate the end-of-frame condition to the error checker, and detect framing error included in the error information; an integrator coupled between the error checker and the controller, and coupled between the framing circuit and the controller, especially, wherein the integrator is configured to determine the error rate determined by counting the occurrence of the error during a period of time and included in the error information.

Substantially regarding claim 36, the prior art of record fails to disclose the signal router for routing information over the network, which comprises the switching matrix having a first number of inputs and a second number of outputs, the error detector coupled to one of the second number of outputs and configured to generate error information by virtue of being configured to

detect errors in the information stream and the controller coupled to the switching matrix and the error detector is configured to select one of the first number of inputs from the first number of inputs, receive error information from the error detector, and configure the switching matrix to couple one of the first number of inputs to one of the second number of outputs, and the switching matrix is configured to receive information stream at one of the first number of inputs, wherein the information stream comprises a plurality of frames and the error detector comprises the error checker coupled to the switching matrix and the controller is configured to generate error check information included in the error information, and the framing circuit coupled to the switching matrix, the controller, and the error checker, and configured to detect the start-of-frame condition for each one of the plurality of frames, indicate the start-of-frame condition to the error checker, detect the end-of-frame condition for each one of the plurality of frames, indicate the end-of-frame condition to the error checker, and detect framing error included in the error information; the error checker and the framing circuit, especially, are coupled to the error counter configured to maintain the error count by virtue of being configured to count the occurrence of the error detected by one of the error checker and the framing circuit, and reset the error count upon the error count being read, the controller is configured to periodically read the error count from the error counter, and calculate an error rate based on the error count in the error information.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kusano (U.S.5,459,718), **Aoki et al.** (U.S.5,453,990) and **Caldara et al.** (U.S.6,208,667) are all cited to show devices and methods for improving the switch's error detection in the communication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-3900.

Tri H. Phan
September 25, 2003

DARGTON
PRIMARY EXAMINER